APPENDIX

- 9. A semiconductor device precursor comprising:
 - a semiconductor substrate;
- a layer of silicon dioxide formed on said semiconductor substrate, said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of metal contaminants; and
- a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.
- 10. A field effect transistor comprising:
 - a semiconductor substrate;
- a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;
- a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and
- a source, a drain and a gate formed in said semiconductor substrate to form a field effect transistor.
- 11. A memory array comprising:
 - a semiconductor substrate;
- a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

Serial No. 09/605,293 Docket No. MIO 0037 VA

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; and

a gate, a source and a drain for each of said field effect transistors formed on said semiconductor substrate.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

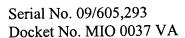
a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology; and

a repeating series of gates, sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of gates, sources and drains being formed on said semiconductor substrate.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of metal contaminants;



a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of a insulating material formed on at least a portion of said layer of polycrystalline silicon;

a source region and a drain region formed on said layer of polycrystalline silicon; and a gate electrode formed on said layer of insulating material.